1/5 Inch 2 Mega CMOS Image Sensor
SP2518

Specification

Version Commercial 1.7
2012.03.26

SuperPix Micro Technology Co., Ltd
SuperPix™ SP2518 image sensor is one of SuperPix™ 2 Mega Digital image sensor series products. These series sensors have the same maximum image format, UXGA, which means they can be adapted by lots of different kinds of portable equipment, for instance, mobile phones or notebooks. The SP2518 is the newest one of this series, which is based on the 3rd generation 1.75um CMOS image sensor pixel architecture designed by SuperPix™, offering high performance images, making it an ideal choice for mainstream phones. An additional SPI function let SP2518 can access image data from other sensor, which make it can be capable of multi-sensor products.

**Functionalities**
- CMOS Image Sensor
- Image Signal Processor

**Applications**
- Mobile Phone
- Notebook
- PC-Cam
- Web-Cam
- Digital Camera
- Toys

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Overview

General Description

SuperPix™ SP2518 image sensor is one of SuperPix™ 2-megapixel Digital image sensor series products. These series sensors have the same maximum image format, UXGA, which means they can be adapted by lots of different kinds of portable equipment, for instance, mobile phones or notebooks. The SP2518 is the newest one of this series, which is based on the 3rd generation 1.75um CMOS image sensor pixel architecture designed by SuperPix™, offering high performance images, making it an ideal choice for mainstream phones. An additional SPI function let SP2518 can access image data from other sensor, which make it can be capable of multi-sensor products. When it works with SuperPix™ SP0827, they can provide high cost performance dual sensor solution.

A high performance system on a chip (SOC) sensor, SP2518 is a chip built on SuperPix™ proprietary pixel and ISP technology for the users who demand high quality sensor for multiple realms. SP2518’s image signal processor module includes automatic exposure control, gain control, white balance, black level calibration, lens correction, defect pixel canceling and more. Additionally, it also features all standard image quality controls such as color saturation, hue, gamma, sharpness (edge enhancement) and noise cancellation. Camera controls are accessed over a standard serial camera control bus interface. Other key image processing features include binning functionality that minimizes spatial artifacts and removes image artifacts around edges to deliver clean, crisp images, critical for achieving best-in-class 2-megapixel images. Moreover, SuperPix™’s proprietary sensor technology utilizes advanced algorithms to cancel Vertical Fixed Pattern Noise (VFPN), eliminate smearing, and drastically reduce blooming.

Extending the company’s portfolio of 2-megapixel sensor, the 1.75um pixel architecture enables the SP2518 to offer high performance imaging and high definition video in an ultra-compact 1/5 inch optical format, making it an ideal choice for mainstream handset equipments. The advanced pixel architecture
delivers excellent low-light performance for the next generation of high performance mobile phones or PCs.

SP2518 operates at high frame rates, offering SVGA resolution at 30 frames per second (fps), and UXGA resolution at 12 frames per second (fps). SP2518 comes with a standard serial I²C interface and a high speed parallel output interface delivering RAW or YUV or RGB image data.

An overview of the SP2518 Image Sensor features and functions will be given below.

**Function Diagram**

![Function Diagram](image)

**Typical Application List**

- Mobile Phone
- Notebook
- PC-Cam
- Web-Cam
- Digital Camera
- Toys

**Typical Application Diagram**

![Typical Application Diagram](image)
## Key Performance Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Pixel Array</td>
<td>1600 x 1200</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>1.75um x 1.75um</td>
</tr>
<tr>
<td>Active Image Size</td>
<td>2.91 mm x 2.17mm</td>
</tr>
<tr>
<td>Lens Size</td>
<td>1/5 inch</td>
</tr>
<tr>
<td>Power Supply</td>
<td>I/O 1.8V ~ 3.0V</td>
</tr>
<tr>
<td></td>
<td>Core 1.2 VDC ± 5%</td>
</tr>
<tr>
<td></td>
<td>Analog 2.6V ~ 3.0V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>Active 220 mW</td>
</tr>
<tr>
<td></td>
<td>Standby 60 uA</td>
</tr>
<tr>
<td>Output Data format</td>
<td>Raw Bayer Format</td>
</tr>
<tr>
<td></td>
<td>YUV422</td>
</tr>
<tr>
<td></td>
<td>RGB565</td>
</tr>
<tr>
<td>Max Working Clock</td>
<td>62MHz</td>
</tr>
<tr>
<td>Max. Frame Rate</td>
<td>13fps@1600 x 1200 Mode</td>
</tr>
<tr>
<td></td>
<td>30fps@1280 x 720 Mode</td>
</tr>
<tr>
<td></td>
<td>47fps@800 x 600 Mode</td>
</tr>
<tr>
<td></td>
<td>30fps@Binning Mode</td>
</tr>
<tr>
<td>Dark Current @ 60°C</td>
<td>40ele/sec</td>
</tr>
<tr>
<td>SNR max</td>
<td>38dB</td>
</tr>
<tr>
<td>Shutter</td>
<td>Rolling shutter</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-20°C ~ 70°C</td>
</tr>
<tr>
<td>Stable Temperature</td>
<td>0°C ~ 50°C</td>
</tr>
<tr>
<td>Package</td>
<td>COB / TSV</td>
</tr>
</tbody>
</table>

Table 1  Key Performance Parameters
Features List

- Active pixel array 1600 x 1200
- Support for UXGA, SVGA
- Analog gain rage is 1.0x – 15.5x
- The image can be zoomed in and zoomed out from 1600 x 1200 to 60 x 60
- Support for video operations
- Support for horizontal and vertical sub-sample
- Embedded black level control
- Support R, Gr, B, Gb 4 transmission channel in analog portion
- Support VFPN reduction circuit
- Embedded image preprocessor functionality
  - Interpolation arithmetic
  - Bad pixel detection and cancellation
  - Auto white balance
  - Auto exposal control
  - Auto black level calibration
  - Image sharpening
  - Smooth inhibiting noise
  - Color space transform
  - Color saturation control
  - Hue control
  - Programmable gamma control
  - Lens correction
  - Defective pixel canceling
  - Noise canceling
- I²C bus controlling registers inside chip
- Support maximum 62MHz working clock
- Support Globe digital gain control
- Pipeline ADC output 10bit image data
- Support strobe signal in order to control flash lamp
- Support SPI interface data access
Function Description

Pixel Array Structure

The SP2518 pixel array is configured as 1608 columns by 1208 rows, shown below. There are 1600 columns by 1200 rows of optically active pixels.
Image Signal Process

Black Level Compensation

Image signal processor starts the image processing stream with black level compensation module. The Black level compensation module provides the function which is to adjust the black level of the image from the sensor automatically.

Lens Shading Correction

Lens shading correction unit is used to correct the brightness near the edge of the lens, and make the brightness across the field of view similar. SP2518 has an embedded lens shading correction module that can be programmed to precisely counter the shading effect of a lens on each RGB color signal. The Lens Shading Correction module multiplies RGB signals by a 2-dimensional correction function \( F(x,y) \), whose profile in both \( x \) and \( y \) direction is a piecewise quadratic polynomial with coefficients independently programmable for each direction and color.

Bad Pixel Correction

Bad pixels will be detected and be replaced by a value calculated from the neighbor
pixel during the Bad Pixel module.

**Smooth and Sharpness**

In this module, smoothing is used to remove the noise in planes and sharpness is used to enhance the edges and detail regions. This block is designed especially for images taken outdoors. The sharpness module of SP2518 is integrated in the color interpolation module.

**Color Interpolation**

Color interpolation module is to convert the raw data to RGB image data. The algorithm is a digital image process used to interpolate a complete image from the partial raw data received from the color filter in form of a matrix of colored pixels. Each 10-bit raw pixel data is converted to RGB value using an edge-sensitive color interpolation algorithm.

**Auto White Balance**

Auto white balance unit is help to remove the unrealistic color from the image automatically by referencing the white balance pre-gain. With auto white balance unit, the still / video camera system can determine the color temperature of the light and automatically adjust for the color temperature.

**Color Correction**

Color correction unit is design to correct the color with the color correction coefficient. The color correction multiplies the interpolated RGB value by programmable 3x3 matrix to map the color response of the sensor to a desired target. The matrix values are determined based on the spectral response and the cross talk characteristics of the sensor and the values can be programmable. This module can deliver vivid images for users.

**Gamma Correction**

The SP2518 includes a module for gamma correction that has the capability to adjust its gamma curve, to enhance the performance under certain lighting conditions. As a result, the images turn to more fresh after this module.
RGB to YUV

After the gamma correction, the image data stream undergoes RGB to YUV conversion. The RGB format image data can be turned to YUV422 format.

I²C Bus

Single READ and Single WRITE

The SP2518 I²C write address is 60H and read address is 61H. A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device’s 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a WRITE and a 1 indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

Two figures that is shown below will illustrate SP2518 single READ sequence and single WRITE sequence.
Figure 5  I2C Read & Write Description
Data Bit Transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock – it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The SP0838 will hold the value of the SDA pin to logic 0 during the logic 1 state of the Acknowledge clock pulse on SCLK.

Data Valid

The master must ensure that data is stable during the logic 1 state of the SCLK pin. All transitions on the SDA pin can only occur when the logic level on the SCLK pin is “0”.

Figure 6  I²C Acknowledge Bit Description

Figure 7  I²C Data Transport Description
### Timing Parameter

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fscl</td>
<td>SBCL clock frequency</td>
<td>0</td>
<td>400</td>
<td>KHz</td>
</tr>
<tr>
<td>tbuf</td>
<td>Bus free time between a stop and a start</td>
<td>1.2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>thd_sta</td>
<td>Hold time for a repeated start</td>
<td>1</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>tlow</td>
<td>LOW period of SBCL</td>
<td>1.2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>thigh</td>
<td>HIGH period of SBCL</td>
<td>1</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>tsu_sta</td>
<td>Setup time for a repeated start</td>
<td>1.2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>thd_dat</td>
<td>Data hold time</td>
<td>1.3</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>tsu_dat</td>
<td>Data Setup time</td>
<td>250</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>tr</td>
<td>Rise time of SBCL, SBDA</td>
<td>-</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>tf</td>
<td>Fall time of SBCL, SBDA</td>
<td>-</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>tsu_sto</td>
<td>Setup time for a stop</td>
<td>1.2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Cb</td>
<td>Capacitive load of bus line (SBCL, SBDA)</td>
<td>-</td>
<td>-</td>
<td>pf</td>
</tr>
</tbody>
</table>

*Figure 8  I²C Bus Timing Parameter Illustration*
Electric Characteristics

DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD</td>
<td>Power supply voltage for IO and analog</td>
<td>2.6</td>
<td>2.8</td>
<td>3.0</td>
<td>V</td>
</tr>
<tr>
<td>VDDIO</td>
<td>Power supply voltage for IO and digital</td>
<td>1.6</td>
<td>1.8</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input high voltage</td>
<td>0.7xVDDIO</td>
<td></td>
<td>3.0</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input low voltage</td>
<td>0</td>
<td></td>
<td>0.3xVDDIO</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output high voltage @ 8mA</td>
<td>0.7xVDDIO</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output low voltage @ 8mA</td>
<td>0.3xVDDIO</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>T</td>
<td>Junction Temperature</td>
<td>-20</td>
<td>25</td>
<td>70</td>
<td>°C</td>
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</tbody>
</table>

Examination Item

<table>
<thead>
<tr>
<th>No.</th>
<th>Reliability Items</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Temp Cycle</td>
<td>-20°C  ~ 70°C each 30 min, 24 cycles</td>
</tr>
<tr>
<td>2</td>
<td>High Temp. &amp; Humidity storage</td>
<td>70°C / 80% / 72Hr</td>
</tr>
<tr>
<td>3</td>
<td>Low Temp. &amp; Humidity storage</td>
<td>-20°C / 96Hr natural dry, for 3 hours</td>
</tr>
<tr>
<td>4</td>
<td>High Temp Operating</td>
<td>70°C / 80% / 72Hr / 2.8V other pins are active condition</td>
</tr>
<tr>
<td>5</td>
<td>Low Temp Operating</td>
<td>-20°C / 72Hr / 2.8V other pins are active condition</td>
</tr>
<tr>
<td>6</td>
<td>Drop Test</td>
<td>1.5m drop, 1 X 6 plane (Camera with 100g cradle)</td>
</tr>
<tr>
<td>7</td>
<td>Random Vibration</td>
<td>5~100HZ, 3 axis (X,Y,Z),15min[axis],swing :6mm</td>
</tr>
</tbody>
</table>
Package

Top View
(bumps down)

Slide View
Figure 9  Pin Name
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Nominal</th>
<th>Min.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Body Dimension X</td>
<td>A</td>
<td>4105</td>
<td>4080</td>
<td>4130</td>
</tr>
<tr>
<td>Package Body Dimension Y</td>
<td>B</td>
<td>4259</td>
<td>4234</td>
<td>4284</td>
</tr>
<tr>
<td>Package Height</td>
<td>C</td>
<td>730</td>
<td>670</td>
<td>790</td>
</tr>
<tr>
<td>Ball Height</td>
<td>C1</td>
<td>130</td>
<td>100</td>
<td>160</td>
</tr>
<tr>
<td>Package Body Thickness</td>
<td>C2</td>
<td>600</td>
<td>565</td>
<td>635</td>
</tr>
<tr>
<td>Thickness of glass surface to wafer</td>
<td>C3</td>
<td>445</td>
<td>425</td>
<td>465</td>
</tr>
<tr>
<td>Ball Diameter</td>
<td>D</td>
<td>250</td>
<td>220</td>
<td>280</td>
</tr>
<tr>
<td>Total Ball count</td>
<td>N</td>
<td>42</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>pin pitch X axis</td>
<td>J1</td>
<td>625</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Pin pitch Y axis</td>
<td>J2</td>
<td>550</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Edge to Pin Center Distance along X</td>
<td>S1</td>
<td>490</td>
<td>460</td>
<td>520</td>
</tr>
<tr>
<td>Edge to Pin Center Distance along Y</td>
<td>S2</td>
<td>479.5</td>
<td>450</td>
<td>510</td>
</tr>
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</table>

Figure 10  Package Dimensions

<table>
<thead>
<tr>
<th>PIN#</th>
<th>PAD_NAME</th>
<th>I/O</th>
<th>Description</th>
<th>PIN#</th>
<th>PAD_NAME</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>DVDD28</td>
<td>DP</td>
<td>Digital I/O Power 2.8V</td>
<td>D5</td>
<td>DVDD15</td>
<td>DP</td>
<td>Digital core power 1.5V, internal only</td>
</tr>
<tr>
<td>A3</td>
<td>DGND</td>
<td>DG</td>
<td>Digital Ground</td>
<td>D6</td>
<td>AGND28</td>
<td>AG</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>A4</td>
<td>PCLK</td>
<td>O</td>
<td>Pixel Output Clock</td>
<td>D7</td>
<td>DVDD28</td>
<td>DP</td>
<td>Digital I/O Power 2.8V</td>
</tr>
<tr>
<td>A5</td>
<td>DGND</td>
<td>DG</td>
<td>Digital Ground</td>
<td>E1</td>
<td>DVDD28</td>
<td>DP</td>
<td>Digital I/O Power 2.8V</td>
</tr>
<tr>
<td>A6</td>
<td>DVDD28</td>
<td>DP</td>
<td>Digital I/O Power 2.8V</td>
<td>E2</td>
<td>ECLK</td>
<td>I</td>
<td>Input Clock</td>
</tr>
<tr>
<td>B1</td>
<td>D[1]</td>
<td>O</td>
<td>Pixel Array Output Bit 1</td>
<td>E3</td>
<td>BYP_LDO</td>
<td>I</td>
<td>&quot;0&quot;Internal Power,&quot;1&quot;External Power</td>
</tr>
<tr>
<td>B3</td>
<td>D[3]</td>
<td>O</td>
<td>Pixel Array Output Bit 3</td>
<td>E5</td>
<td>AGND28</td>
<td>AG</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>B5</td>
<td>D[7]</td>
<td>O</td>
<td>Pixel Array Output Bit 7</td>
<td>F1</td>
<td>SDBA</td>
<td>I/O</td>
<td>Slave Tri-state,I2C Data Bus</td>
</tr>
<tr>
<td>C1</td>
<td>DVDD18</td>
<td>DP</td>
<td>Digital Power 1.8V</td>
<td>F3</td>
<td>SCLK</td>
<td>I</td>
<td>Slave I2C Clock Bus</td>
</tr>
<tr>
<td>C2</td>
<td>STROBE</td>
<td>O</td>
<td>Strobe Signal</td>
<td>F4</td>
<td>NC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>D[4]</td>
<td>O</td>
<td>Pixel Array Output Bit 4</td>
<td>F5</td>
<td>AGND28</td>
<td>AG</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>C4</td>
<td>HSYNC</td>
<td>O</td>
<td>Horizontal Sync Signal</td>
<td>F6</td>
<td>AVDD28</td>
<td>AP</td>
<td>Analog power 2.8V</td>
</tr>
<tr>
<td>C5</td>
<td>D[8]</td>
<td>O</td>
<td>Pixel Array Output Bit 8</td>
<td>G1</td>
<td>AVDD28</td>
<td>AP</td>
<td>Analog power 2.8V</td>
</tr>
<tr>
<td>C6</td>
<td>CVDD28</td>
<td>CP</td>
<td>Charge-pump power 2.8V</td>
<td>G2</td>
<td>AGND28</td>
<td>AG</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>D1</td>
<td>DGND</td>
<td>DG</td>
<td>Digital Ground</td>
<td>G3</td>
<td>PVD28</td>
<td>PP</td>
<td>Pixel Power 2.8V</td>
</tr>
<tr>
<td>D2</td>
<td>DVDD15</td>
<td>DP</td>
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Figure 11  Pin Description
## Revision History

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